

Description

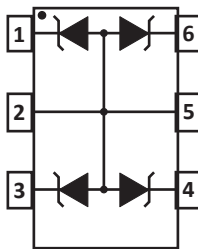
The DCxx44S2 are subminiature monolithic TVS suppressor arrays designed for the protection of sensitive IC components from the damaging effects of Electrostatic Discharge(ESD). These devices are ideally suited for use in portable electronics such as SMART phones, laptops, and other wireless devices.

The DCxx44S2 are usable on I/O ports where the signal voltage is positive. These devices will also provide protection in accordance with IEC 61000-4-2 and IEC 61000-4-4 requirements. These devices are available in a SOT23-6 package configuration and is rated at 350W peak pulse power(8/20µs) per line.

Mechanical Characteristics

- ◆ Molded JEDEC SOT23-6 Package
- ◆ Approximate Weight: 16 milligrams
- ◆ Lead -Free Pure -Tin Plating (Annealed)
- ◆ Solder Reflow Temperature:
Pure -Tin -Sn, 100: 260-270°C
- ◆ 8mm Tape and Reel Per EIA Standard 481
- ◆ Flammability Rating UL 94V-0

Dimensions and Pin Configuration



Circuit and Pin Schematic

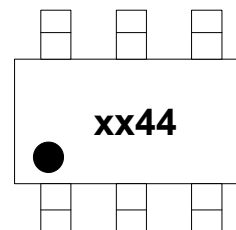
Features

- ◆ Compatible with IEC 61000-4-2 (ESD): Air ±30KV, Contact ±30KV
- ◆ Compatible with IEC 61000-4-4 (EFT): 40A, 5/50ns
- ◆ 350W Peak Pulse Power per line (tp=8/20µs)
- ◆ Monolithic Design
- ◆ Protects 4 lines
- ◆ Unidirectional and Bidirectional Configurations
- ◆ ESD Protection > 25 kilovolts
- ◆ Low Clamping Voltage
- ◆ Low Leakage Current
- ◆ Available in Multiple Voltages
- ◆ RoHS Compliant
- ◆ REACH Compliant

Applications

- ◆ SMART Phones
- ◆ Portable Electronics
- ◆ FireWire, Ethernet and USB Interfaces

Marking Information



xx44 = Device Marking Code
Dot denotes Pin1

Ordering Information

Part Number	Marking	Packaging	Reel Size
DCxx44S2	xx44	3000/Tape & Reel	7 inch

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power(8/20 μs)	Ppk	350	W
Operating Temperature Range	T _L	-55 to +150	$^\circ\text{C}$
Storage Temperature Range	T _{stg}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise specified)

DC3344S2 (Marking Code:3344)						
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	VRWM			3.3	V	
Breakdown Voltage	VBR	4			V	I _T = 1mA
Reverse Leakage Current	I _R			0.5	μA	VRWM = 3.3V
Forward Voltage	V _F		0.8	1.2	V	I _F =10mA
Clamping Voltage	V _C		5		V	I _{PP} = 1A (8 x 20 μs pulse)
Clamping Voltage	V _C		10		V	I _{PP} = 32A (8 x 20 μs pulse)
Peak Pulse Current	I _{PP}			32	A	t _p =8/20 μs
Junction Capacitance	C _J			160	pF	V _R = 0V, f = 1MHz

Note:

1. Test between pin 1 to 2 or 5, 4 to 2 or 5, 6 to 2 or 5, 3 to 2 or 5.
2. Capacitance measured between pins 1, 3, 4, 6 to 2.

DC0544S2 (Marking Code: 0544)						
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V_{RWM}			5	V	
Breakdown Voltage	V_{BR}	6			V	$I_T = 1\text{mA}$
Reverse Leakage Current	I_R			0.5	μA	$V_{RWM} = 5\text{V}$
Forward Voltage	V_F		0.8	1.2	V	$I_F = 10\text{mA}$
Clamping Voltage	V_C		7		V	$I_{PP} = 1\text{A}$ (8 x 20 μs pulse)
Clamping Voltage	V_C		11		V	$I_{PP} = 26\text{A}$ (8 x 20 μs pulse)
Peak Pulse Current	I_{PP}			26	A	$t_p = 8/20\mu\text{s}$
Junction Capacitance	C_J			150	pF	$V_R = 0\text{V}$, $f = 1\text{MHz}$

DC0844S2 (Marking Code: 0844)						
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V_{RWM}			8	V	
Breakdown Voltage	V_{BR}	8.5			V	$I_T = 1\text{mA}$
Reverse Leakage Current	I_R			0.5	μA	$V_{RWM} = 8\text{V}$
Forward Voltage	V_F		0.8	1.2	V	$I_F = 10\text{mA}$
Clamping Voltage	V_C		10		V	$I_{PP} = 1\text{A}$ (8 x 20 μs pulse)
Clamping Voltage	V_C		15		V	$I_{PP} = 20\text{A}$ (8 x 20 μs pulse)
Peak Pulse Current	I_{PP}			20	A	$t_p = 8/20\mu\text{s}$
Junction Capacitance	C_J			130	pF	$V_R = 0\text{V}$, $f = 1\text{MHz}$

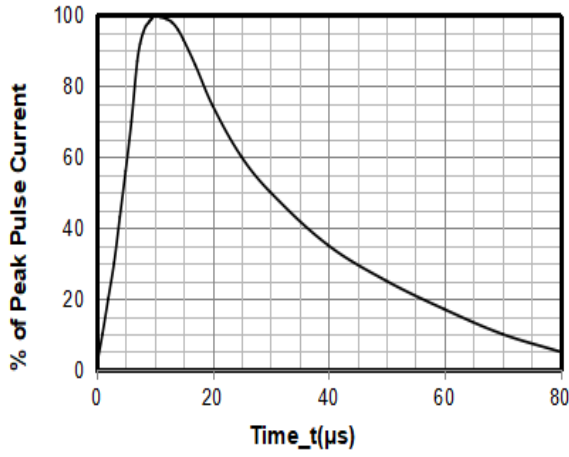
DC1244S2 (Marking Code: 1244)						
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V_{RWM}			12	V	
Breakdown Voltage	V_{BR}	13.3			V	$I_T = 1\text{mA}$
Reverse Leakage Current	I_R			0.5	μA	$V_{RWM} = 12\text{V}$
Forward Voltage	V_F		0.8	1.2	V	$I_F = 10\text{mA}$
Clamping Voltage	V_C		15		V	$I_{PP} = 1\text{A}$ (8 x 20 μs pulse)
Clamping Voltage	V_C		24		V	$I_{PP} = 15\text{A}$ (8 x 20 μs pulse)
Peak Pulse Current	I_{PP}			15	A	$t_p = 8/20\mu\text{s}$
Junction Capacitance	C_J			70	pF	$V_R = 0\text{V}$, $f = 1\text{MHz}$

DC1544S2 (Marking Code: 1544)						
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V_{RWM}			15	V	
Breakdown Voltage	V_{BR}	16.7			V	$I_T = 1\text{mA}$
Reverse Leakage Current	I_R			0.5	μA	$V_{RWM} = 15\text{V}$
Forward Voltage	V_F		0.8	1.2	V	$I_F = 10\text{mA}$
Clamping Voltage	V_C		20		V	$I_{PP} = 1\text{A}$ (8 x 20 μs pulse)
Clamping Voltage	V_C		30		V	$I_{PP} = 12\text{A}$ (8 x 20 μs pulse)
Peak Pulse Current	I_{PP}			12	A	$t_p = 8/20\mu\text{s}$
Junction Capacitance	C_J			60	pF	$V_R = 0\text{V}$, $f = 1\text{MHz}$

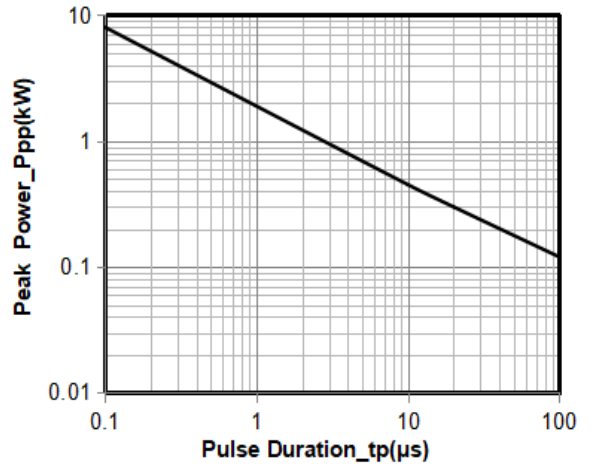
DC2444S2 (Marking Code: 2444)						
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	VRWM			24	V	
Breakdown Voltage	VBR	26.7			V	IT = 1mA
Reverse Leakage Current	IR			0.5	μA	VRWM = 24V
Forward Voltage	VF		0.8	1.2	V	IF=10mA
Clamping Voltage	VC		33		V	I _{PP} = 1A (8 x 20μs pulse)
Clamping Voltage	VC		45		V	I _{PP} = 6A (8 x 20μs pulse)
Peak Pulse Current	I _{PP}			6	A	tp=8/20μs
Junction Capacitance	CJ			35	pF	VR = 0V, f = 1MHz

DC3644S2 (Marking Code: 3644)						
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	VRWM			36	V	
Breakdown Voltage	VBR	40			V	IT = 1mA
Reverse Leakage Current	IR			0.5	μA	VRWM = 36V
Forward Voltage	VF		0.8	1.2	V	IF=10mA
Clamping Voltage	VC		41		V	I _{PP} = 1A (8 x 20μs pulse)
Clamping Voltage	VC		60		V	I _{PP} = 4A (8 x 20μs pulse)
Peak Pulse Current	I _{PP}			4	A	tp=8/20μs
Junction Capacitance	CJ			20	pF	VR = 0V, f = 1MHz

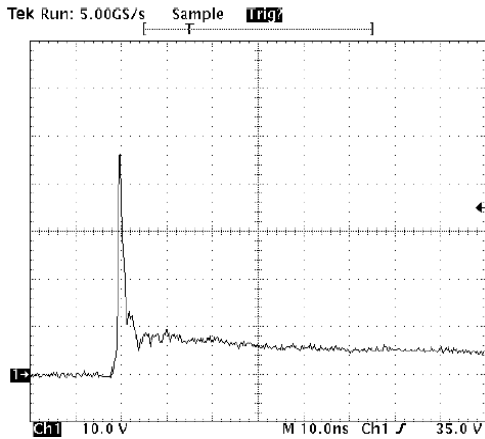
Typical Performance Characteristics (TA=25°C unless otherwise Specified)



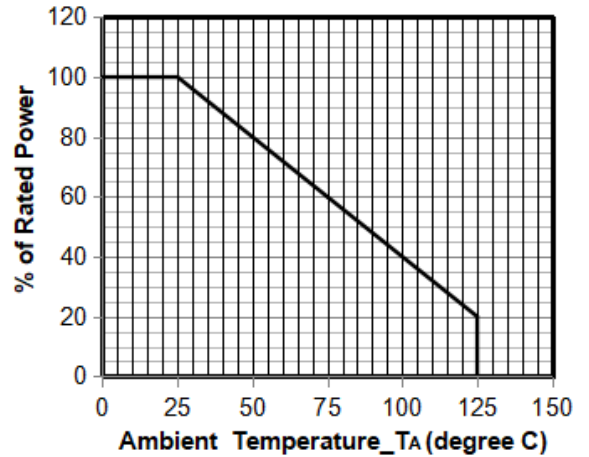
8 X 20μs Pulse Waveform



Peak Pulse Power vs. Pulse Time

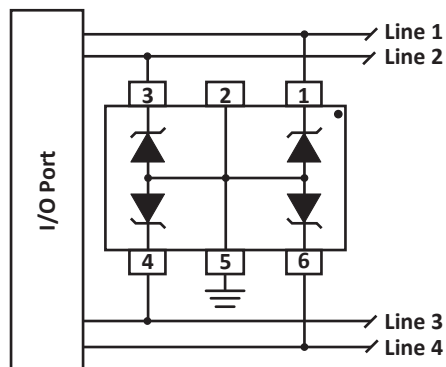


Note: Data is taken with a 10x attenuator
ESD Clamping Voltage
8 kV Contact per IEC61000-4-2



Power Derating Curve

Application Information



Common-Mode I/O Port Protection

Circuit connectivity is as follows:

- Line 1 connected to pin 1.
- Line 2 connected to pin 3.
- Line 3 connected to pin 4.
- Line 4 connected to pin 6.
- Pin 5 connected to ground.
- Pin 2 not connected.

Circuit Board Recommendations

Circuit board layout is critical for electromagnetic compatibility protection. The following guidelines are recommended: The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.

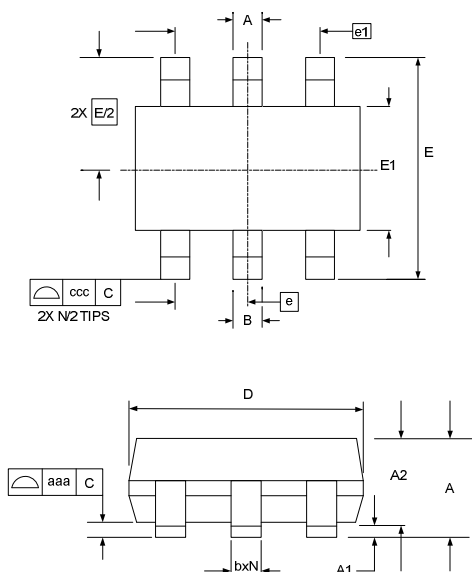
The path length between the TVS device and the protected line should be minimized.

All conductive loops including power and ground loops should be minimized.

The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.

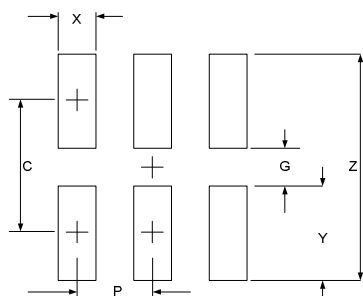
Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

SOT23-6 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90		1.45	0.035		0.057
A1	0.00		0.15	0.000		0.006
A2	0.90	1.15	1.30	0.035	0.045	0.051
b	0.25		0.50	0.010		0.020
c	0.08		0.22	0.003		0.009
D	2.80	2.90	3.10	0.110	0.114	0.122
E1	1.50	1.60	1.75	0.060	0.063	0.069
E	2.80 BSC			0.110 BSC		
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
N	6			6		
aaa	0.10			0.004		
ccc	0.20			0.008		

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	2.50	0.098
G	1.40	0.055
P	0.95	0.037
X	0.60	0.024
Y	1.10	0.043
Z	3.60	0.141

Contact Information

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